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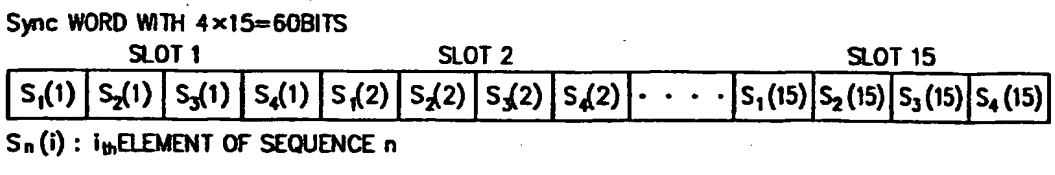

(57) Abstract: There is provided a method of synchronizing received sync frames to reference sync frames. Each of the received sync frames and the reference sync frames has a sync word and is divided into a predetermined number of slots and each slot is divided into a plurality of bits. In the method, a frame sync word is provided to have a first correlation when the reference sync frames are synchronized with the received sync frames and a second correlation different from the first correlation when the received sync word is shifted version of the reference sync word by one of the two specific numbers of slots, for example, such as (5) or (10).

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APPARATUS AND METHOD FOR GENERATING SYNC WORD AND TRANSMITTING AND RECEIVING THE SYNC WORD IN W-CDMA COMMUNICATION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to an apparatus and method for generating a sync word and verifying the frame sync word in a CDMA (Code Division Multiple Access) communication system, and in particular, to an apparatus and method for generating a sync word and verifying the sync word in an asynchronous CDMA (W-CDMA) communication system.

2. Description of the Related Art

As the third-generation mobile communication is under standardization, efforts are expended toward the integration of mobile communication systems around the world.

Especially, harmonization of the North America synchronous CDMA (CDMA 2000) and the European W-CDMA(Universal Mobile Terrestrial System) is accelerated. In the course, the chip rate of 4.096Mcps in W-CDMA is expected to be reduced to 3.84Mcps. Therefore, the W-CDMA system should be partially reconfigured in such a way that it can operate at a chip rate reduced to a 15/16 (3.84Mcps/4.096Mcps) of the original chip rate of 4.096Mcps. That is, whereas one frame includes 16 slots in a conventional W-CDMA communication system, one frame will have 15 slots in an integrated W-CDMA communication system. Therefore, the best way of designing the integrated W-CDMA system is considered to reduce 16 slots per frame to 15 slots per frame without any modification to a slot structure.

The change in the number of slots per frame for harmonization between CDMA 2000 and W-CDMA is accompanied by a design modification to a pilot

sync word pattern for use in frame synchronization verification.

The W-CDMA radio communication standards under development in the 3GPP (3rd Generation Partnership Project) as of May 1999, one of conventional W-CDMA communication system technologies, involves frame synchronization verification using a sync word. The sync word in the conventional technology is designed on the assumption that one frame has 16 slots. Now, a new sync word fit for a 15 slots per frame structure is under development. With 15 slots per frame, a conventional synchronization verification method based on the 16 slot-per-frame structure is not applicable to the W-CDMA system. Hence, a new synchronization verification method is required to fit the 15 slots-per-frame structure.

SUMMARY OF THE INVENTION

A first object of the present invention is therefore to provide an apparatus and method for generating a sync word in a W-CDMA communication system.

A second object of the present invention is to provide an apparatus and method for generating a frame sync word in a W-CDMA communication system in which one frame has 15 slots and each slot includes a plurality of sync bits.

A third object of the present invention is to provide an apparatus and method for generating a sync word which has a first correlation at frame synchronization and a second correlation at least two slot positions of a frame period where frames are asynchronous by specific slots in a W-CDMA communication system.

A fourth object of the present invention is to provide an apparatus and method for generating a sync word which has a first correlation being the highest correlation at frame synchronization, a second correlation being the smallest correlation at at least two slot positions of a frame period where frames are asynchronous by specific slots, and a third correlation when frames are asynchronous in a different condition from the above two conditions in a W-CDMA communication system.

A fifth object of the present invention is to provide an apparatus and method for generating a sync word which is formed with at least two sequences with length 2^P-1 (P is a positive integer) generated by a sync word generator and has a first correlation being the highest correlation at frame synchronization, a second correlation being the smallest correlation at at least two slot positions of a frame period where frames are asynchronous by specific slots, and a third correlation at any other slot position of the frame period where frames are asynchronous in a W-CDMA communication system.

A sixth object of the present invention is to provide an apparatus and method for generating and transmitting a sync word which is formed with at least two sequences and has a first correlation being the highest correlation when the two sequences start at the same point, a second correlation being the smallest correlation at two predetermined offsets, and a third correlation between the first and second correlations at any other offset in a W-CDMA communication system.

A seventh object of the present invention is to provide an apparatus and method for transmitting a sync word which has a first correlation being the highest correlation at the same start point, a second correlation being the smallest correlation at two predetermined offsets, and a third correlation between the first and second correlations at any other offset by a transmitter and acquiring frame synchronization using the sync word by a receiver in a W-CDMA communication system.

Briefly, these and other objects can be achieved by providing a method of verifying synchronization of received frame by correlating the sync word position bits included in the received frame to reference sync word. Each of the received frame have a sync word and is divided into a predetermined number of slots and each slot having a plurality of bits including sync bits. In the method, a frame sync word is provided to have a first correlation value when the reference sync word are synchronized with the received sync word and a second correlation value different from the first correlation value when the received sync word is shifted version of the reference sync word by one of the two specific numbers of slots, for example, such as 5or 10.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

FIGs. 1A, 1B, and 1C are concept views of frame synchronization in a W-CDMA communication system;

FIGs. 2A to 2D illustrate the slot structure of each channel in the W-CDMA communication system;

FIGs. 3A to 3H illustrate the pilot structure of each channel in the W-CDMA communication system;

FIGs. 4A, 4B, and 4C illustrate sync word structures in the W-CDMA communication system;

FIG. 5 illustrates a relationship among a frame, slots, pilots, and a sync word in connection with FIGs. 1 to 4C;

FIG. 6 illustrates the structure of a sync word used in a W-CDMA communication system according to an embodiment of the present invention;

FIG. 7 is a flowchart illustrating a sync word generating procedure according to the embodiment of the present invention;

FIG. 8 is a graph showing a correlation characteristic of a sync word configured as shown in FIG. 6;

FIG. 9 is a block diagram of a transmitting device in the W-CDMA communication system according to the embodiment of the present invention;

FIG. 10 is a block diagram of a receiving device in the W-CDMA communication system according to the embodiment of the present invention;

FIG. 11 illustrates an embodiment of a sync word generator in the receiving device shown in FIG. 10;

FIG. 12 illustrates another embodiment of the sync word generator in the receiving device shown in FIG. 10;

FIGs. 13A and 13B are block diagrams of a frame synchronization verifier in the receiving device shown in FIG. 10; and

FIG. 14 is a flowchart illustrating a synchronization verifying procedure in the receiving device shown in FIG. 10.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described herein below with reference to the accompanying drawings. In the following description, well-known functions or constructions are not described in detail since they would obscure the invention in unnecessary detail.

Verification of a sync word pattern and synchronization according to the feature of the present invention is applicable to a CDMA mobile communication system, especially a W-CDMA communication system. The present invention specifically relates to use of a sync word for synchronization verification. Here, the sync word is a bit sequence in a specific pattern known to both a transmitter and a receiver. Although the sync word pattern is usually predetermined and stored in the transmitter and receiver, it is generated during an actual operation and communicated between the transmitter and the receiver.

Synchronization is considered in three ways: PN chip synchronization, slot synchronization, and frame synchronization, which implies that a receiver operates in synchronization with a transmitter over time by providing a signal transmitted by the transmitter in PN chip units, slot units, or frame units. An embodiment of the present invention provides an apparatus and method for generating a sync word for use in verification of frame (basic transmission unit) synchronization. The frame synchronization verification is performed after acquisition of PN chip, slot (frame segment), and frame synchronization. To do so, the transmitter transmits a sync bit in the slots of a frame and the receiver calculates a correlation of an autonomously generated sync word to the received bits positioned in the sync word to verify frame synchronization. If frames are not in synchronization, the synchronization acquisition process is repeated. In the alternative, if frames are in synchronization, a received frame is demodulated and decoded to thereby obtain the information. This will be described later referring to FIG. 14.

Now a description of frame synchronization will be given herein below. FIGs. 1A, 1B, and 1C are concept views of frame synchronization in a W-CDMA communication system. In the drawings, slots are numbered 1 to 15, implying that one frame has 15 slots.

Referring to FIGs. 1A, 1B, and 1C, each upper frame provides the time of a sync word in a received frame and each lower frame provides the time of an autonomously generated reference sync word in a receiver. FIG. 1A illustrates the case that the reception time of the frame sync word from a transmitter is equal to the time of the autonomously generated reference sync word; the two frames are in synchronization. FIGs. 1B and 1C illustrate the cases that the reception time of the frame sync word from a transmitter is different from the time of the autonomously generated reference sync word; the two frames are not in synchronization. Here, it is assumed that slots are synchronized even though frames are asynchronous, as shown in FIGs. 1B and 1C. When frames are asynchronous by a multiple of one slot as shown in FIGs. 1B and 1C, the number of the slots are defined as an offset. For example, the offsets are 0, +1, and −5 respectively in FIGs. 1A, 1B, and 1C. An offset of 15 or a multiple of 15 is equivalent to an offset of 0. An offset with a negative sign (−) can be correlated to an offset of a positive sign (+). For example, an offset of −5 can be correlated to an offset of +10.

FIGs. 2A to 2D illustrate the position and bit number of a pilot in a slot of each channel according to the 3GPP W-CDMA radio standards which are under development. The pilot on each channel is an unmodulated spread signal which provides a basis for coherent demodulation used for channel estimation.

FIG. 2A illustrates the slot structure of an uplink dedicated physical control channel (DPCCH) with a 5 to 8-bit pilot in an earlier part of each slot. A pilot is in a latter part of each slot, occupying 4, 8, or 16 bits on a downlink dedicated physical channel (DPCH) in FIG. 2B. FIG. 2C illustrates the slot structure of a downlink primary common control physical channel (PCCPCH). Here, the pilot is in a latter part of each slot, occupying 8 bits. On a downlink secondary common control physical channel (SCCPCH), the pilot is 8 or 16 bits in a latter part of each slot in FIG. 2D.

Part of the pilot bits in the slot structures shown in FIGs. 2A to 2D can be used to form a sync word. Bits in one slot among bits used to form a sync word are defined as a sync symbol(sync bits). Sync bits in one slot form one sync symbol and sync symbols in the slots of one frame form one sync word.

FIGs. 3A to 3H illustrate sync bits among pilot bits in a specific slot of each channel as provided by the 3GPP W-CDMA radio standards. Blank bits in FIGs. 3A to 3H are pilot bits having the same value in all slots, that is, bits other than sync bits. These pilot bits are referred to as typical pilot bits. Black-marked bits are sync bits having particular values in different slots for use in verifying frame synchronization. The pilot bits are all or partially used for channel estimation.

Four (4) pilot bits of a 5 to 8-bit pilot signal are used as sync bits in one slot of an uplink DPCCH in FIGs. 3A to 3D. In FIGs. 3E and 3F, 2 of 4 pilot bits and 2 of 4 diversity bits in one slot of a downlink DPCH are used as sync bits. FIG. 3G illustrates an 8-bit pilot with 4 sync bits in one slot of a downlink DPCH, PCCPCH, or SCCPCH. In FIG. 3H, 8 of 16 pilot bits are used as sync bits in one slot of a downlink DPCH or SCCPCH.

The positions and number of sync bits in a frame are shown in FIGs. 2A to 2D and FIGs. 3A to 3H by way of example for the better understanding of the embodiment of the present invention. Therefore, it is obvious that other slot structures and bit arrangements can be contemplated within the scope and spirit of the present invention.

As described above, the embodiment of the present invention provides a generally applied sync word pattern and a method and apparatus for generating the sync word pattern in a W-CDMA communication system where one frame includes 15 or 2^P-1 (P is a positive integer) slots. For clarity of description, the following description of the embodiment of the present invention is conducted on the assumption that one frame is comprised of 15 slots.

FIGs. 4A, 4B, and 4C illustrate different sync words formed out of sync bits in the slots of one frame.

In FIG. 4A, one sync symbol is 2 bits and one sync word includes 30 bits (=2x15). FIG. 4B illustrates a sync symbol of 4 bits and thus a sync word of 60 bits (=4x15). With 8-bit sync symbols, a sync word has 120 bits (=8x15) in FIG.

4C. The sync words shown in FIGs. 4A, 4B, and 4C occur repeatedly in every frame.

FIG. 5 illustrates a relationship among a frame, slots, pilots, and a sync word on an uplink DPCCH using a 6-bit pilot signal as shown in FIG. 3B, for example. Referring to FIG. 5, one frame has 15 slots (see FIG. 1), one slot includes a pilot and information data (see FIG. 2), the pilot has sync bits and typical pilot bits (see FIG. 3), and a sync word is formed out of the sync bits in one frame (see FIG. 4).

FIG. 6 illustrates a sync word pattern for a 60-bit sync word according to the embodiment of the present invention.

Referring to FIG. 6, let the bit number of a sync symbol be N and the period of the sync word (sync word length) is 15N. If N is 4, the sync word length is 60 bits.

As shown in FIG. 6, a sync word is formed out of N sequences with period 15. Each sequence is comprised of sync bits at the same positions in the slots of one frame and thus has a period 15 (i.e., the number of slots).

If an i^{th} element of an n^{th} sequence among the N sequences is $S_n(i)$, the sync symbols in 15 slots are listed as below.

(Table 1)

sync symbol in 1^{st} slot: $S_1(1), S_2(1), ..., S_N(1)$
sync symbol in 2^{nd} slot: $S_1(2), S_2(2), ..., S_N(2)$
sync symbol in 3^{rd} slot: $S_1(3), S_2(3), ..., S_N(3)$
sync symbol in 4^{th} slot: $S_1(4), S_2(4), ..., S_N(4)$
sync symbol in 5^{th} slot: $S_1(5), S_2(5), ..., S_N(5)$
sync symbol in 6^{th} slot: $S_1(6), S_2(6), ..., S_N(6)$
sync symbol in 7^{th} slot: $S_1(7), S_2(7), ..., S_N(7)$
sync symbol in 8^{th} slot: $S_1(8), S_2(8), ..., S_N(8)$
sync symbol in 9^{th} slot: $S_1(9), S_2(9), ..., S_N(9)$
sync symbol in 10^{th} slot: $S_1(10), S_2(10), ..., S_N(10)$

sync symbol in 11th slot: $S_1(11), S_2(11), ..., S_N(11)$
sync symbol in 12th slot: $S_1(12), S_2(12), ..., S_N(12)$
sync symbol in 13th slot: $S_1(13), S_2(13), ..., S_N(13)$
sync symbol in 14th slot: $S_1(14), S_2(14), ..., S_N(14)$
sync symbol in 15th slot: $S_1(15), S_2(15), ..., S_N(15)$

For N = 4 in FIG. 5, the sync word is depicted in Table 2.

(Table 2)

sync symbol in 1st slot: $S_1(1), S_2(1), S_3(1), S_4(1)$
sync symbol in 2nd slot: $S_1(2), S_2(2), S_3(2), S_4(2)$
sync symbol in 3rd slot: $S_1(3), S_2(3), S_3(3), S_4(3)$
sync symbol in 4th slot: $S_1(4), S_2(4), S_3(4), S_4(4)$
sync symbol in 5th slot: $S_1(5), S_2(5), S_3(5), S_4(5)$
sync symbol in 6th slot: $S_1(6), S_2(6), S_3(6), S_4(6)$
sync symbol in 7th slot: $S_1(7), S_2(7), S_3(7), S_4(7)$
sync symbol in 8th slot: $S_1(8), S_2(8), S_3(8), S_4(8)$
sync symbol in 9th slot: $S_1(9), S_2(9), S_3(9), S_4(9)$
sync symbol in 10th slot: $S_1(10), S_2(10), S_3(10), S_4(10)$
sync symbol in 11th slot: $S_1(11), S_2(11), S_3(11), S_4(11)$
sync symbol in 12th slot: $S_1(12), S_2(12), S_3(12), S_4(12)$
sync symbol in 13th slot: $S_1(13), S_2(13), S_3(13), S_4(13)$
sync symbol in 14th slot: $S_1(14), S_2(14), S_3(14), S_4(14)$
sync symbol in 15th slot: $S_1(15), S_2(15), S_3(15), S_4(15)$

The above sync word is generated in the following way.

Step 1: step 2 is repeated for slot number i = 1 to 15;
Step 2: step 3 is repeated for bit number n = 1 to N in a slot; and
Step 3: the sync bit $S_n(i)$ is output.

The sync word generation method is expressed in a flowchart shown in FIG. 7.

Referring to FIG. 7, for generation of the sync word, slot index i is set to 1

in step 711 and sync index n in slot #1 is set to 1 in step 713. A sync bit $S_n(i)$ is output in step 715 and sync index n is incremented by 1 in step 717. If n is 4 or smaller, the procedure goes back to step 715. If n is larger than 4 in step 719, slot index i is incremented by 1 in step 721. If slot index i is larger than 15, slot index i is set to the initial value 1 back in step 711 and the above procedure is repeated. If slot index i is 15 or smaller, sync index n is set to the initial value 1 back in step 713 to generate sync bits in the next slot and the above procedure is repeated.

The sync word can be generated as a combination of a plurality of sequences in the above manner or as one whole sequence. The sync word has correlation characteristics to facilitate sync detection.

The sync word generated in the operation shown in FIG. 7 exhibits an auto-correlation characteristic as illustrated in FIG. 8.

Referring to FIG. 8, if frames are in synchronization, that is, a slot offset is 0 or a multiple of 15, the auto-correlation of the sync word is the highest value, 15N. This is referred to as a first correlation 811. In the case of asynchronous frames, that is, a slot offset other than 0 or a multiple of 15, the auto-correlation of the sync word is a third correlation 813 between the highest value 15N and the lowest value –P or a second correlation value 812 –P. Here, P is a value greater than 0. The correlation value is –P at two positions on an axis representing 15 possible offsets. In the embodiment of the present invention, the correlation of the sync word is –P for offsets of 5 and 10.

Sequences of a sync word showing the above correlation characteristic are generated in the way described below.

All sequences with length 15, that is, 32768 sequences are checked in terms of auto-correlation characteristics and 572 correlation types are achieved. All possible correlation type pairs are produced from the 572 correlation types. The correlations of sequences of each correlation type pair at each offset are added. Correlation type pairs are selected which have a minimum number of the lowest points, small absolute values of the correlation values at offsets other than an offset showing the smallest correlation. Table 3 lists sequences of length 15 which are

such correlation type pairs as selected in the above procedure and their correlations. Due to the large number of possible sequences of individual correlation types, Table 3 is limited to four sequences.

(Table 3)

	Sequence	Correlation Type (Offsets 0 to 14)
S^1	110110110000000 011011011000000 001101101100000 000110110110000 000011011011000	15, 3, −1, 7, −1, −5, −1, −5, −5, −1, −5, −1, 7, −1, 3
S^2	111010101110000 111100010101000 011101010111000 101010001111000 011110001010100	15, −1, 3, −9, −1, −5, 3, 3, 3, 3, −5, −1, −9, 3, −1
S^3	111010011000000 110010111000000 011101001100000 011001011100000 001110100110000	15, 3, −1, −1, −1, −5, −1, 3, 3, −1, −5, −1, −1, −1, 3
S^4	101011011001000 100110110101000 110110101000100 110111010100100 010101101100100	15, −5, −1, 3, 3, −5, −1, −1, −1, −1, −5, 3, 3, −1, −5

In Table 3, sequences S^1 and S^2 and sequences S^3 and S^4 are correlation type pairs selected in the above method. The correlation types of S^1 and S^2 at the offsets are [15, 3, −1, 7, −1, −5, −1, −5, −5, −1, −5, −1, 7, −1, 3] and [15, −1, 3, −9, −1, −5, 3, 3, 3, 3, −5, −1, −9, 3, −1], respectively. The correlations of the sequences at each offset are added to produce [30, 2, 2, −2, −2, −10, 2, −2, −2, 2, −10, −2, −2, 2, 2]. As noted from FIG. 8, a first correlation being the highest 30 is at an offset of 0 or a multiple of 15, a second correlation being the lowest −10 is at offsets of 5 and 10, and a third correlation 2 or −2 having a very small absolute

value is at the other offsets.

The correlation types of S^3 and S^4 at the offsets are [15, 3, −1, −1, −1, −5, −1, 3, 3, −1, −5, −1, −1, −1, 3] and [15, −5, −1, 3, 3, −5, −1, −1, −1, −1, −5, 3, 3, −1, −5], respectively. The correlations of the sequences at each offset are added to produce [30, −2, −2, 2, 2, −10, −2, 2, 2, −2, −10, 2, 2, −2, −2]. The correlation is the lowest −10 at offsets of 5 and 10 and a very small absolute value, 2 or −2 at the other offsets in this case, too.

From a plurality of correlation type pairs selected in the above-described manner, two correlation type pairs are selected, and their correlations are added at each offset. Then, a frame code word is obtained which shows the correlation characteristic shown in FIG. 8. When a frame sync word is formed with the sequences S^1 and S^2, and S^3 and S^4 shown in Table 3, the highest correlation (first correlation 30) appears at slot offset 0 in one frame period with 15 slots, the lowest correlation at slot offset 5 or 10 (second correlation −10), and other correlations (a third correlation 2 or −2) at the other slot offsets.

The correlation types of the sequences S^1 and S^2, and S^3 and S^4 at the offsets are [30, 2, 2, −2, −2, −10, 2, −2, −2, 2, −10, −2, −2, 2, 2] and [30, −2, −2, 2, 2, −10, −2, 2, 2, −2, −10, 2, 2, −2, −2], respectively. The correlations at each offset are added and then the above correlation characteristic is exhibited. That is, a sync word of length 60 having the correlation characteristic shown in FIG. 8 is formed by alternately outputting the four sequences of Table 3 bit by bit.

While a sync word with four bits per slot is described by way of example, sync bits per slot can be 2, 4, or 8 bits as shown in FIG. 3. If a sync word has 2 bits per slot, one sequence of S^1 and S^2, or one sequence of S^3 and S^4 are selected for use. If a sync word has four bits per slot, one sequence is selected from each of the sequences S^1, S^2, S^3, and S^4 or two sequences are selected from each pair of S^1 and S^2, and S^3 and S^4. If a sync word has eight bits per slot, two sequences are selected from each of S^1, S^2, S^3, and S^4 or two pairs of four sequences are selected from each pair of S^1 and S^2, and S^3 and S^4.

The same correlation characteristic as shown in FIG. 8 can be achieved by

delaying the sequences of Table 3 by the same bit units. That is, the same correlation characteristic is shown at the offsets of corresponding sequences when the sequences S^1 and S^2 are delayed by the same bit units or the sequences S^3 and S^4 are delayed by the same units. Therefore, a sync word having the correlation characteristic shown in FIG. 8 can be generated by delaying sequences S^1 and S^2, and S^3 and S^4 of correlation type pairs satisfying the condition described earlier at the output terminal of a sync word generator 1023, shown in FIG. 10.

Accordingly, when sync words of the structure shown in Table 3 are used, an autonomously generated reference sync word in a receiving device is in frame synchronization with the sync word of a received frame as shown in FIG. 1A (slot offset is 0 or a multiple of 15), the correlation of the sync words is the first value, 15N as indicated by 811 in FIG. 8. If frames are not in synchronization as shown in FIGs. 1B and 1C, the first correlation is not obtained. In this case, when a slot offset is neither 0 nor a multiple of 5 as shown in FIG. 1B, the correlation of the sync words is a third correlation being 0 as indicated by 813 in FIG. 8. If the slot offset is not 0 but is a multiple of 5 (other than 15 or a multiple thereof), the correlation of the sync words is a second correlation being –P as indicated by 812 in FIG. 8. That is, with asynchronous frames, different correlations are obtained according to slot offsets.

Frame synchronization is verified in a receiving device by calculating and analyzing a correlation. If the calculated correlation is the first correlation 811, it is determined that frames are in synchronization. If the calculated correlation is the third correlation 813, one slot is shifted and a correlation is calculated at the next slot. Then, if the second correlation 812 is detected, the frame synchronization verifying operation is performed while shifting every five slots until the first correlation 811 is detected. Therefore, the use of a sync word having such a correlation characteristic increases reliability with which frame synchronization is verified and allows rapid synchronization utilizing the relation between the first and second correlations when frames are asynchronous.

The following is a description of the structures and operations of a transmitting device and a receiving device for transmitting and receiving a sync word in a W-CDMA communication system according to an embodiment of the

present invention.

FIG. 9 is a block diagram of a data channel transmitting device for generating a sync word and transmitting the sync word in a base station or a mobile station according to the embodiment of the present invention.

Referring to FIG. 9, a sync word generator 911, which will be described later in detail in connection with FIGs. 12, and 13, generates a sync symbol of N sync bits in each slot to generate a sync word, that is, a sync word with 15N sync bits. A controller 921 generates a first select signal sel1 to select the sync bits received from the sync word generator 911 and typical pilot bits in a pilot period of each slot and a second select signal sel2 to select the pilot and other data in each slot. Since pilot periods are different on different uplink and downlink channels as shown in FIGs. 3A to 3H, the controller 921 generates the first select signal sel1 for selecting sync bits and typical pilot bits to be inserted into a pilot period in each slot of a corresponding channel according to one of the sync bit and typical pilot bit patterns shown in FIGs. 3A to 3H. The controller 921 generates the second select signal sel2 for selecting the position of the pilot information in each slot of the corresponding channel according to one of the pilot information location patterns shown in FIGs. 2A to 2D. The selected pilot information is inserted into a different position in a slot depending on uplink and downlink channels as shown in FIGs. 2A to 2D. A first selector 913 multiplexes the sync bits received from the sync word generator 911 and the typical pilot bits in response to the first select signal sel1 according to one of the corresponding patterns shown in FIGs. 3A to 3H. A second selector 915 multiplexes the pilot received from the first selector 913 and other data in response to the second select signal sel2 according to one of the corresponding patterns shown in FIGs. 2A to 2D. The first and second selectors 913 and 915 can be multiplexers. A spreader 917 spreads slot information received from the second selector 915.

A transmitting device in a basestation (BS) further has a sync channel transmitter which is later described. Sync information is transmitted via primary and secondary sync channels (P-SCH and S-SCH) or only via the P-SCH. The structure and operation of a sync channel transmitter is disclosed in Korea Application No. 99-15332 and Korea Application No. 99-18921.

FIG. 10 is a block diagram of a receiving device for receiving sync words in a base station or a mobile station according to the embodiment of the present invention. A sync word generator 1023 in FIG. 10 is the same as the sync word generator 911 of FIG. 9 in configuration and generates a sync word having the same characteristics.

In FIG. 10, a synchronizer 1013 acquires PN chip, slot, and frame synchronization from a received signal. The synchronizer 1013 is disclosed in detail in Korea Application No. 99-15332 and Korea Application No. 99-18921. The synchronizer can be provided in a mobile station or a base station. The synchronizer 1013, according to the embodiment of the present invention, provides a timing control signal and information about the state of a sync word to a sync word generator 1023 from the acquired synchronization. The timing control signal controls the output time point of the sync word generator 1023. The sync word state information indicates a position of a sync word to be output from the sync word generator 1023 at a specific time point.

Referring to FIG. 10, the sync word generator 1023 receives the timing control signal and the sync word state information from the synchronizer 1013 and generates a sync word having the characteristic shown in FIG. 8 under the control of a sync word generation controller 1021. The sync word generated by the sync word generator 1023 is compared with the sync word in a received frame and the comparison result is used as information for frame synchronization.

FIGs. 11 and 12 are block diagrams of the sync word generator 1023 and other peripheral devices, showing their relationship according to the embodiment of the present invention. A sync word sequence generated from the sync word generator 1023 has a period of 15 slots, i.e., one frame, and thus 15N sync bits are output for one frame period. Therefore, the sync word is output in the pattern shown in FIG. 6 with the correlation characteristic shown in FIG. 8.

FIG. 11 illustrates the sync word generator 1023 including a memory 1100 for storing a sync word. Referring to FIG. 11, the sync word generator 1023 receives sync word size information N from the sync word generation controller

1021, accesses N bits in each slot and 15N bits in one frame based on the sync word size information, and outputs them as a sync word. The sync word generator 1023 receives the timing control signal and the sync word state information from the synchronizer 1013 and outputs the sync bits of the sync word at given positions at a given time point.

FIG. 12 illustrates another embodiment of the sync word generator 1023. The sync word generator 1023 is a memory for storing sync word and outputting them when necessary

In FIG. 10, a despreader 1011 despreads received channel signals based on synchronization information received from the synchronizer 1013. A multiplexing controller 1015 generates a control signal for separating and selecting a pilot and other data from a corresponding channel among slot signals in the structures shown in FIGs. 2A to 2D. A demultiplexer 1017 demultiplexes a pilot and other data of a corresponding channel among pilot signals of sync bit patterns shown in FIGs. 3A to 3H in a despread slot in response to the select signal received from the controller 1015. Here, the demultiplexer 1017 reversely performs the operation of the second selector 916 shown in FIG. 9. A sync word extractor 1019 extracts sync bits from a pilot in each slot. That is, the sync word extractor 1019 extracts the sync bits marked black among pilot bits shown in FIGs. 3A to 3H. The sync word extractor 1019 performs the reverse operation of the first selector 913 shown in FIG. 9. The operation of the sync word extractor 1019 can be performed under the control of the controller 1015.

A frame synchronization verifier 1025 receives the sync bits from the sync word extractor 1019 and a sync word from the sync word generator 1023 and verifies frame synchronization. FIG. 13A is a block diagram of the frame synchronization verifier 1025. The embodiment of the present invention uses two thresholds TH1 and TH2 by way of example. In this case, the frame synchronization verifier 1025 calculates a correlation, compares the correlation with TH1 and TH2 (TH1 > TH2), and outputs the comparison result in two bits. Here, TH1 is used as reference data for detecting the first correlation 811 of FIG. 8, and TH2 is used as reference data for detecting the second correlation 812 of FIG. 8.

FIG. 13A is a block diagram of the frame synchronization verifier 1025 according to the embodiment of the present invention. The frame synchronization verifier 1025 receives sync words from the sync word extractor 1019 and the sync word generator 1023, multiples the sync word bit by bit, accumulates the resulting values for one frame, and calculates the correlation of the two sync words. A determiner 1315 in the frame synchronization verifier 1025 determines from the correlation whether frames have been synchronized and a specific offset has occurred. The determiner 1315 may include a plurality of deciders 1351 and 1353 (multiple threshold devices) as shown in FIG. 13B. Then, the determiner 1315 determines whether the correlation is greater than TH1 (frame synchronization), neither greater than TH1 nor smaller than TH2 (non-synchronization and a slot offset not being a multiple of 5), or smaller than TH2 (non-synchronization and a slot offset being a multiple of 5).

Referring to FIG. 13A, the frame synchronization verifier 1025 receives the sync words from the sync word extractor 1019 and the sync word generator 1023 and generates a frame synchronization verification signal. A multiplier 1311 multiplies the sync words bit by bit. An accumulator 1313 accumulates the output of the multiplier 1311 on a frame by frame basis and calculates a correlation between the sync words. The determiner 1315 determines whether frames have been synchronized from the correlation. FIG. 13B illustrates an embodiment of the determiner 1315. The determiner 1315 compares the output of the accumulator 1313 with TH1 and TH2 to thereby determine whether frame synchronization has been acquired.

Referring to FIG. 13B, the first threshold TH1 is smaller than the first correlation 811 and greater than the third correlation 813. The second threshold TH2 is smaller than the third correlation 813 and greater than the second correlation 812. A first comparator 1351 compares the correlation received from the accumulator 1313 with the first threshold TH1. If the correlation is greater than the first threshold TH1, the first comparator 1351 generates a true signal, determining that the first correlation 811 has been detected. If the correlation is smaller than the first threshold TH1, the first comparator 1351 generates a false signal. The second comparator 1353 compares the correlation with the second

threshold TH2. If the correlation is smaller than the second threshold TH2, the second comparator 1353 generates a true signal, determining that the second correlation 812 has been detected. If the correlation is greater than the second threshold TH2, the second comparator 1353 generates a false signal. A parallel-to-serial converter (PSC) 1355 outputs signals received from the comparators 1351 and 1353, two bits at a time. Here, upon generation of the true signal in the first comparator 1351, the determiner 1315 outputs a first decision signal, indicating that the first correlation 811 has been detected. Upon generation of the true signal in the second comparator 1353, the determiner 1315 outputs a second decision signal, indicating that the second correlation 812 has been detected. Upon generation of the false signals in both the first and second comparators 1351 and 1353, the determiner 1315 outputs a third decision signal, indicating that the third correlation has been detected.

Therefore, the determiner 1315 generates a decision signal indicating frame synchronization if the correlation output from the accumulator 1313 is greater than the first threshold TH1. A decision signal is generated indicating that frame synchronization has not been acquired and a slot offset is not a multiple of 5 if the correlation is neither greater than the first threshold TH1 nor smaller than the second threshold TH2. A decision signal is generated indicating that frame synchronization has not been acquired and a slot offset is a multiple of 5 if the correlation is smaller than the second threshold TH2.

The frame synchronization verifier 1025 outputs the decision signals to the synchronizer 1013 to control acquisition of frame synchronization.

The above synchronization acquisition method may end after a synchronization verification is performed once in the case of synchronization acquisition, or it can be repeated at predetermined intervals.

FIG. 14 is a flowchart illustrating a synchronization verification and recovery procedure according to an embodiment of the present invention. In step 1411, a receiver first acquires synchronization from a received signal using a synchronizer and, in step 1413, calculates a correlation between the sync word obtained from the received signal and an autonomously generated sync word. Then,

in step 1415, the receiver compares the correlation with the first threshold TH1. If the correlation is greater than the first threshold TH1, the receiver demodulates and decodes a received frame in step 1417, determining that frames are in synchronization. If the correlation is not greater than the first threshold TH1, the receiver in step 1419 compares the correlation with the second threshold TH2 (TH1 > TH2). If the correlation is smaller than the second threshold TH2, the receiver in step 1421 shifts 5 slots from the autonomously generated frame synchronization and then returns to step 1413. If the correlation is not smaller than the second threshold TH2, the receiver shifts the autonomously generated frame sync word by one slot and returns to step 1413. Here, the synchronizer 1023 can shift the autonomously generated frame sync word by changing the sync word state information received from the sync word generator 1023 according to the control signal received from the frame synchronization verifier 1025. The sync word state information provides a position of a sync word sequence to be output at a specific time point. For example, the sync word state information includes information concerning into which offset position the autonomously generated sync word should be placed.

Referring to FIG. 14, upon synchronization acquisition in step 1411, a correlation between sync words is calculated and the acquired frame synchronization is verified in step 1413. If the correlation is greater than the first threshold TH1, the receiver determines that the first correlation 811 has been detected, that is, confirms frame synchronization in step 1415 and demodulates and decodes received frame data in step 1417.

On the other hand, if the correlation is smaller than the first threshold TH1, the receiver compares the correlation with the second threshold TH2 in step 1419. If the correlation is not smaller than the second threshold TH2, the correlation is the third correlation 813 and a slot offset is not a multiple of 5. In this case, the frame synchronization verifier 1025 transmits the third decision signal to the synchronizer 1013 in step 1423. Then, the synchronizer 1013 shifts the autonomously generated sync word by one slot and the procedure goes back to step 1413. If the correlation is smaller than the second threshold TH2 in step 1419, the correlation is the second correlation 812 and a slot offset is the 5^{th} or 10^{th} slot in one frame period. In this case, the frame synchronization verifier 1025 sends the

second decision signal to the synchronizer 1013 in step 1421 and the synchronizer 1013 shifts the autonomously generated sync word by 5 slots. Then, the procedure goes back to step 1413.

In accordance with the embodiment of the present invention, a sync word showing the correlation characteristic of FIG. 8 is used, a receiving device is configured as shown in FIG. 10, and frame synchronization is verified in the procedure of FIG. 14.

In the procedure of FIG. 14, the receiver of FIG. 10 acquires synchronization from an input signal through the synchronizer 1013 in step 1411. It is assumed that the synchronizer 1013 has acquired PN chip and slot synchronization for basic despreading. In the case of successful synchronization acquisition, frames are synchronized.

In step 1413, the receiver calculates a correlation between a sync word obtained from the input signal and an autonomously generated sync word through the frame synchronization verifier 1025 (a correlation including a multiplier and a summing device).

In step 1415, the receiver compares the correlation with the first threshold TH1 using the first comparator of the determiner in the frame synchronization verifier. If frames are in synchronization, this implies that an offset is 0 and the first correlation 811 has been detected, as shown in FIG. 8. If the correlation is greater than the first threshold TH1, the determiner of the frame synchronization verifier 1025 determines that frames are synchronized and sends a synchronization confirm signal (the first decision signal) to the synchronizer 1013. The receiver demodulates and decodes a received frame in step 1417. That is, the receiver obtains information from other data output in FIG. 9. If the correlation is not greater than the first threshold TH1, the receiver goes to step 1419.

In step 1419, the receiver compares the correlation with the second threshold TH2 (TH2 < TH1) using the second comparator of the determiner in the frame synchronization verifier 1025. If frames are asynchronous by 5 or 10 slots, this implies that an offset is 5 or 10 and the second correlation 812, that is, the

lowest correlation has been detected (see FIG. 8). If the correlation is smaller than the second threshold TH2, the determiner in the frame synchronization verifier 1025 determines that frames are asynchronous by 5 or 10 slots and sends a first synchronization amend signal (the second decision signal) to the synchronizer 1013. Then, the receiver shifts the receiver frame sync word by 5 slots in step 1421 and returns to step 1413. If the correlation is not smaller than the second threshold TH2, the determiner determines that the correlation is neither the highest point nor the lowest point, that is, the third correlation 813 and an offset is a value other than any of 0, 5, and 10 (a multiple of 5), and sends a second synchronization confirm signal (the third decision signal) to the synchronizer 1013. The receiver shifts the autonomously generated sync word by one slot by use of the synchronizer 1013 and returns to step 1413.

While two lowest correlation points are shown at offsets 5 and 10 in FIG. 8, a sync word having the lowest correlation points in different positions but similar correlation characteristic can be achieved. With the sync word, synchronization can be verified and recovered within the spirit of the present invention.

A sync word generated in accordance with the present invention as described above, exhibits such correlation characteristic as shown in FIG. 8 due to the nature of sequences in the sync word. At frame synchronization (i.e., offset 0 or a multiple of 15), the auto-correlation of the sync word is 15N. With asynchronous frames and offset not 0 or a multiple of 15, the auto-correlation of the sync word is 0. If frames are asynchronous at an offset of a multiple of 5, the auto-correlation is a specific negative value –P. By use of the sync word, frame synchronization can be verified with high reliability. For example, if the correlation is greater than the first threshold, it is determined that frames are in synchronization and a received frame is demodulated and decoded. If the correlation is smaller than the second threshold (the second threshold < the first threshold), it is determined that a slot offset is a multiple of 5 and synchronization is verified again after a 5-slot shift. If the correlation is between the first and second thresholds, synchronization is re-verified after a one-slot shift. Frame synchronization can be acquired by a maximum of seven occurrences of the above procedure.

While the invention has been shown and described with reference to certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method of verifying synchronization of a received frame by calculating correlation value of a reference sync word and a received sync word included in the frame comprising;

a step of determining synchronization when the correlation value is exceed a first predetermined threshold meaning that the reference sync word are synchronized with the received sync word; and

a step of determining one of the two shifted synchronization when the correlation value is exceed second predetermined threshold value.

2. A sync word generating apparatus in a Code Division Multiple Access (CDMA) communication system where each frame is divided into a plurality of slots, each slot has a plurality of sync symbols, and a frame sync word is formed out of the sync symbols of the plurality of slots, comprising:

a plurality of sequence generators for generating at least two sync symbol sequences which have a first correlation when the reference frame is synchronized with a received frame and a second correlation different from the first correlation when the first slot of the received frame is located at each of at least two slot division points spaced at a predetermined distance over the plurality of slots; and

a selector for multiplexing sync symbols received from the sequence generators and selecting a corresponding multiplexed sync symbol for each slot.

3. The sync word generating apparatus of claim 2, wherein each frame is comprised of 15 slots and the two slot division points are the 5^{th} and 10^{th} slots.

4. The sync word generating apparatus of claim 3, wherein the sync word has a third correlation between the first correlation and the second correlation when the first slot of the received frame is located at a slot division point different from a multiple of 5.

5. The sync word generating apparatus of claim 4, wherein the sync

word has first and second sync symbols in each slot and the apparatus further comprising first and second sequence generators for generating the first and second sync symbols, the first generator generating a first sequence S^1 and the second generator generating a second sequence S^2, wherein S^1 and S^2 are defined as follows:

	sequence
S^1	110110110000000 011011011000000 001101101100000 000110110110000 000011011011000
S^2	111010101110000 111100010101000 011101010111000 101010001111000 011110001010100

6. The sync word generating apparatus of claim 4, wherein the sync word has first and second sync symbols in each slot and the apparatus further comprising first and second sequence generators for generating the first and second sync symbols, the first generator generating a first sequence S^1 and the second generator generating a second sequence S^2, wherein S^1 and S^2 are defined as follows:

	sequence
S^1	111010011000000 110010111000000 011101001100000 011001011100000 001110100110000
S^2	101011011001000 100110110101000 110110101000100 110111010100100 010101101100100

7. The sync word generating apparatus of claim 5, wherein the sync word is used for a downlink dedicated physical channel (DPCH).

8. The sync word generating apparatus of claim 6, wherein the sync word is used for a downlink DPCH.

9. The sync word generating apparatus of claim 4, wherein the sync word has first to fourth sync symbols in each slot and the apparatus further comprising a first sequence generator for generating the first and second sync symbols and a second sequence generator for generating the third and fourth sync symbols, the first generator generating two sequences out of a first sequence S^1 and the second generator generating a second sequence S^2, wherein S^1 and S^2 are defined as follows:

	sequence
S^1	1101101100000000 0110110110000000 0011011011000000 0001101101100000 0000110110110000 0000011011011000
S^2	1110101011100000 1111000101010000 0111010101110000 1010100011110000 0111100010101000

10. The sync word generating apparatus of claim 4, wherein the sync word has first to fourth sync symbols in each slot and the apparatus further comprising a first sequence generator for generating the first and second sync symbols and a second sequence generator for generating the third and fourth sync symbols, the first generator generating two sequences out of a first sequence S^1 and the second generator generating a second sequence S^2, wherein S^1 and S^2 are defined as follows:

	sequence
S^1	1110100110000000 1100101110000000 0111010011000000 0110010111000000 0011101001100000
S^2	1010110110010000 1001101101010000 1101101010001000 1101110101001000 0101011011001000

11. The sync word generating apparatus of claim 4, wherein the sync

word has first to fourth sync symbols in each slot and the apparatus further comprising at least two sequence generators for generating the first and second sync symbols, the sequence generators generating a first sequence S^1 to a fourth sequence S^4, wherein S^1, S^2, S^3 and S^2 are defined as follows:

	sequence
S^1	110110110000000 011011011000000 001101101100000 000110110110000 000011011011000
S^2	111010101110000 111100010101000 011101010111000 101010001111000 011110001010100
S^3	111010011000000 110010111000000 011101001100000 011001011100000 001110100110000
S^4	101011011001000 100110110101000 110110101000100 110111010100100 010101101100100

12. The sync word generating apparatus of claims 9, 10, or 11, wherein the sync word is used for an uplink dedicated physical control channel (DPCCH)

13. The sync word generating apparatus of claims 9, 10 or 11, wherein the sync word is used for a downlink DPCH.

14. The sync word generating apparatus of claims 9, 10, or 11, wherein the sync word is used for a downlink primary common control physical channel (PCCHPCH).

15 The sync word generating apparatus of claims 9, 10 or 11 wherein the sync word is used for a downlink secondary common control physical channel (SCCPCH).

16. The sync word generating apparatus of claim 4 wherein the sync

word has first to eighth sync symbols in each slot and the apparatus further comprising a first sequence generator for generating the first to fourth sync symbols and a second sequence generator for generating the fifth to eighth sync symbols, the first generator generating four sequences from a first sequence S^1 and the second generator generating four sequences from a second sequence S^2, wherein S^1 and S^2 are defined as follows:

	Sequence
S^1	110110110000000 011011011000000 001101101100000 000110110110000 000011011011000
S^2	111010101110000 111100010101000 011101010111000 101010001111000 011110001010100

17 The sync word generating apparatus of claim 4 wherein the sync word has first to eighth sync symbols in each slot and the apparatus further comprising a first sequence generator for generating the first to fourth sync symbols and a second sequence generator for generating the fifth to eighth sync symbols, the first generator generating four sequences from a first sequence S^1 and the second generator generating four sequences from a second sequence S^2, wherein S^1 and $S^2$are defined as follows:

	Sequence
S^1	111010011000000 110010111000000 011101001100000 011001011100000 001110100110000
S^2	101011011001000 100110110101000 110110101000100 110111010100100 010101101100100

18 The sync word generating apparatus of claim 4 wherein the sync word has first to eighth sync symbols in each slot and the apparatus further comprising a first sequence generator for generating the first and second sync

symbols, a second sequence generator for generating the third and fourth sync symbols, a third sequence generator for generating the fifth and sixth sync symbols, and a fourth sequence generator for generating the seventh and eighth sync symbols, the first to fourth sequence generators each generating, respectively, two sequences from of a first sequence S^1 to a fourth sequence S^4, wherein S^1, S^2, S^3 and S^2 are defined as follows:

	Sequence
S^1	1101101100000000 0110110110000000 0011011011000000 0001101101100000 0000110110110000 0000011011011000
S^2	1110101011100000 1111000101010000 0111010101110000 1010100011110000 0111100010101000
S^3	1110100110000000 1100101110000000 0111010011000000 0110010111000000 0011101001100000
S^4	1010110110010000 1001101101010000 1101101010001000 1101110101001000 0101011011001000

19. The sync word generating apparatus of claims 16, 17 or 18 wherein the sync word is used for a downlink DPCH.

20. The sync word generating apparatus of claims 16, 17 or 18, wherein the sync word is used for a downlink SCCPCH.

21. A channel transmission apparatus in a CDMA communication system where each frame is divided into a plurality of slots, each slot has a plurality of sync symbols, and a frame sync word is formed out of the sync symbols of the plurality of slots, comprising:

a sync word generator having a plurality of sequence generators for generating at least two sync symbol sequences which have a first correlation when a reference frame is synchronized with a received frame and a second correlation

different from the first correlation when a first slot of the received frame is located at each of at least two slot division points spaced at a predetermine distance over the plurality of slots, and a selector for multiplexing sync symbols received from the sequence generators and selecting a corresponding multiplexed sync symbol for each slot;

a first selector for multiplexing sync bits received from the sync word generator and pilot bits which are not used for the sync word and inserting the multiplexed bits at a predetermined location of a pilot period in each slot; and

a second selector for generating channel data generated from the pilot bits received from the first selector and other data

22. A method of synchronizing received sync frames to reference sync frames, each of the received sync frames and the reference sync frames having a sync word and being divided into a predetermined number of slots and each slot being divided into a plurality of bits, the method comprising the step of generating a frame sync word having a first correlation when the reference sync frames are synchronized with the received sync frames and a second correlation different from the first correlation when each of the received sync frames starts at at least two slot division points spaced at a predetermined distance over the plurality of slots of each respective reference sync frame.

23. A frame sync verifying apparatus in a CDMA communication system in which each of a received sync frame and a reference sync frame is divided into a predetermined number of slots and has a sync word and each slot is divided into a plurality of bits, the apparatus comprising:

a sync word generator for generating the frame sync word having a first correlation when the reference sync frames are synchronized with the respective received sync frames and a second correlation different from the first correlation when each of the received sync frames starts at at least two slot division points spaced at a predetermined distance over the plurality of slots of each respective reference sync frame;

a sync word extractor for extracting a frame sync word from the received sync frames; and

a frame sync verifier for verifying frame sync by calculating a correlation of the frame sync word extracted from received sync frames to the generated sync

frame word.

24. A frame sync verifying method in a CDMA communication system in which each of a received sync frame and a reference sync frame is divided into a predetermined number of slots and has a sync word and each slot is divided into a plurality of bits and which has a sync word generator for generating the frame sync word having a first correlation when the reference sync frames are synchronized with the received sync frames and a second correlation different from the first correlation when each of the received sync frames starts at at least two slot division points spaced at a predetermined distance over the plurality of slots of each respective reference sync frame, the method comprising the steps of:

extracting a frame sync word from the received sync frame;

determining whether the correlation of the extracted frame sync word to the generated sync word is one of the first correlation and the second correlation;

if a first correlation is determined, determining that frame sync has been acquired;

if a second correlation is determined, shifting the generated frame sync word by a predetermined number of slots and returning to the correlation calculation step; and

if neither the first correlation nor the second correlation is determined, shifting the generated frame sync word by one slot and returning to the correlation calculation-step.

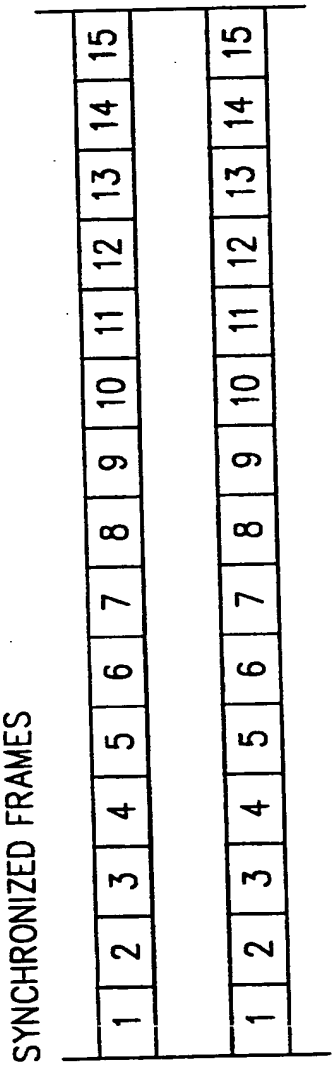
SYNCHRONIZED FRAMES
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

FIG. 1A

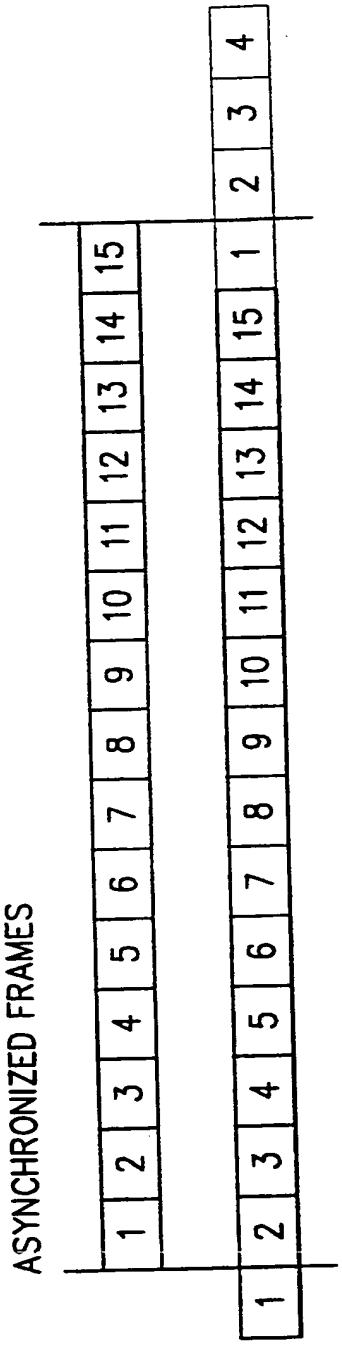
ASYNCHRONIZED FRAMES
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 1 2 3 4

FIG. 1B

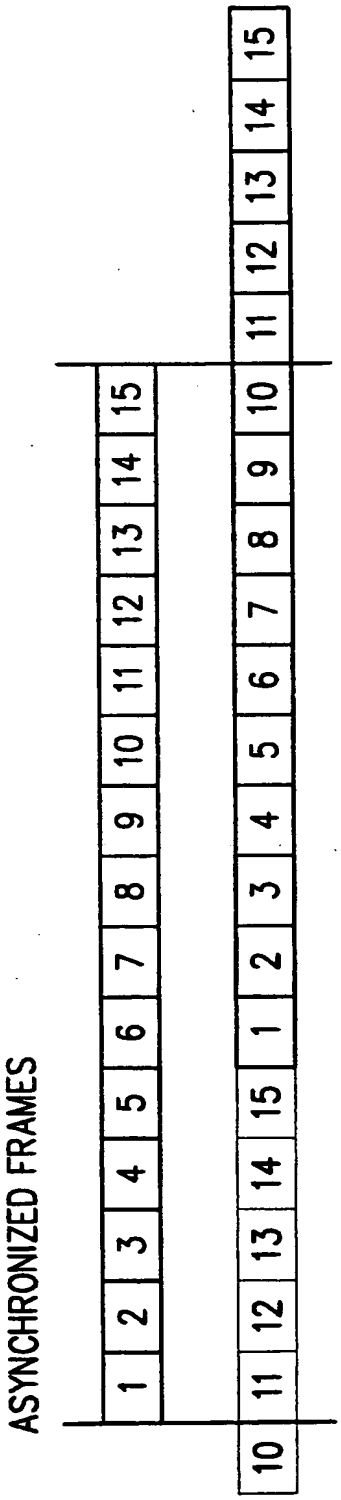
ASYNCHRONIZED FRAMES
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
10 11 12 13 14 15 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

FIG. 1C

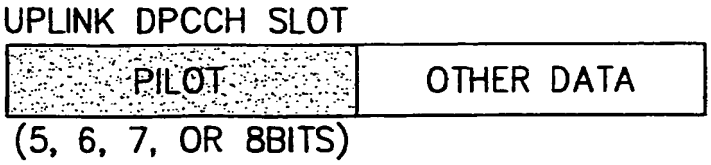

FIG. 2A

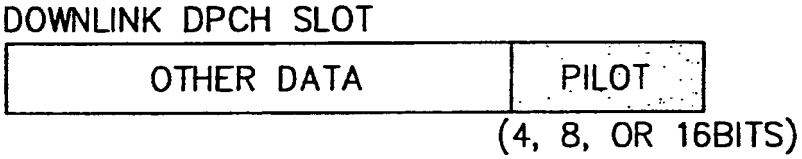

FIG. 2B

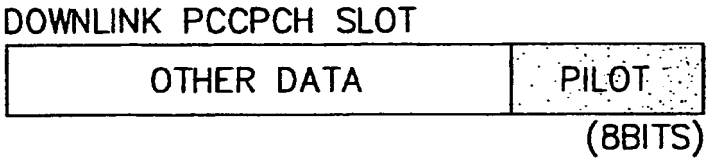

FIG. 2C

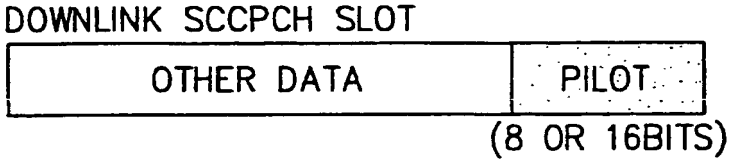

FIG. 2D

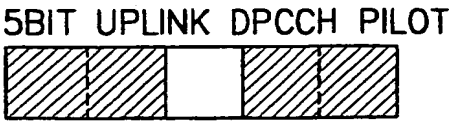

FIG. 3A

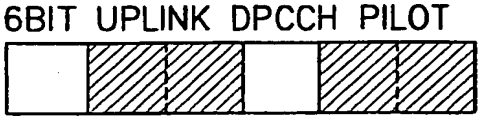

FIG. 3B

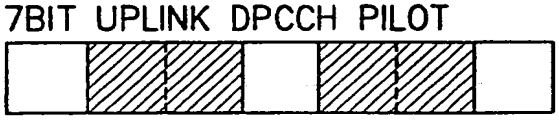

FIG. 3C

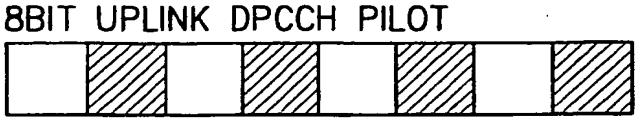

FIG. 3D

4BIT DOWNLINK DPCH PILOT

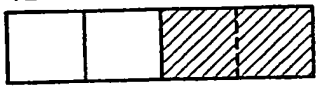

FIG. 3E

4BIT DOWNLINK DPCH PILOT(DIVERSITY ANTENNA)

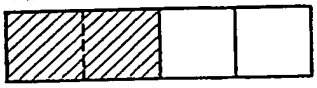

FIG. 3F

8BIT DOWNLINK DPCH PILOT,
COWNLINK PCCPCH PILOT, OR DOWNLINK SCCPCH PILOT

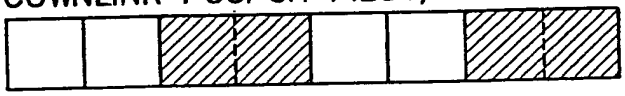

FIG. 3G

16BIT DOWNLINK DPCH PILOT OR DOWNLINK SCCPCH PILOT

FIG. 3H

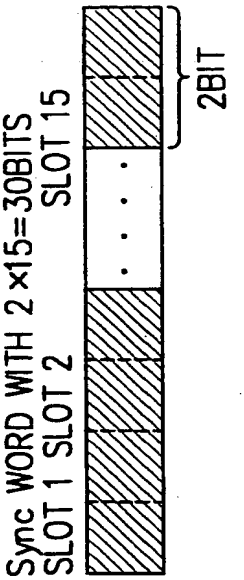

FIG. 4A

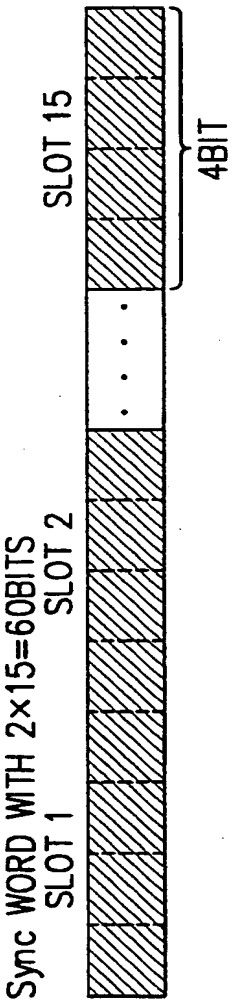

FIG. 4B

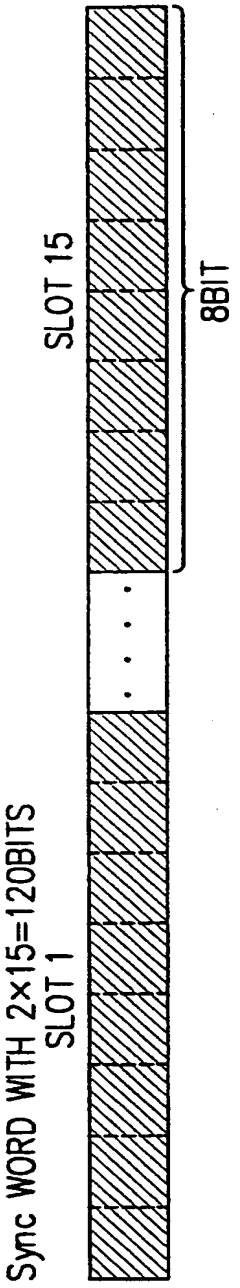

FIG. 4C

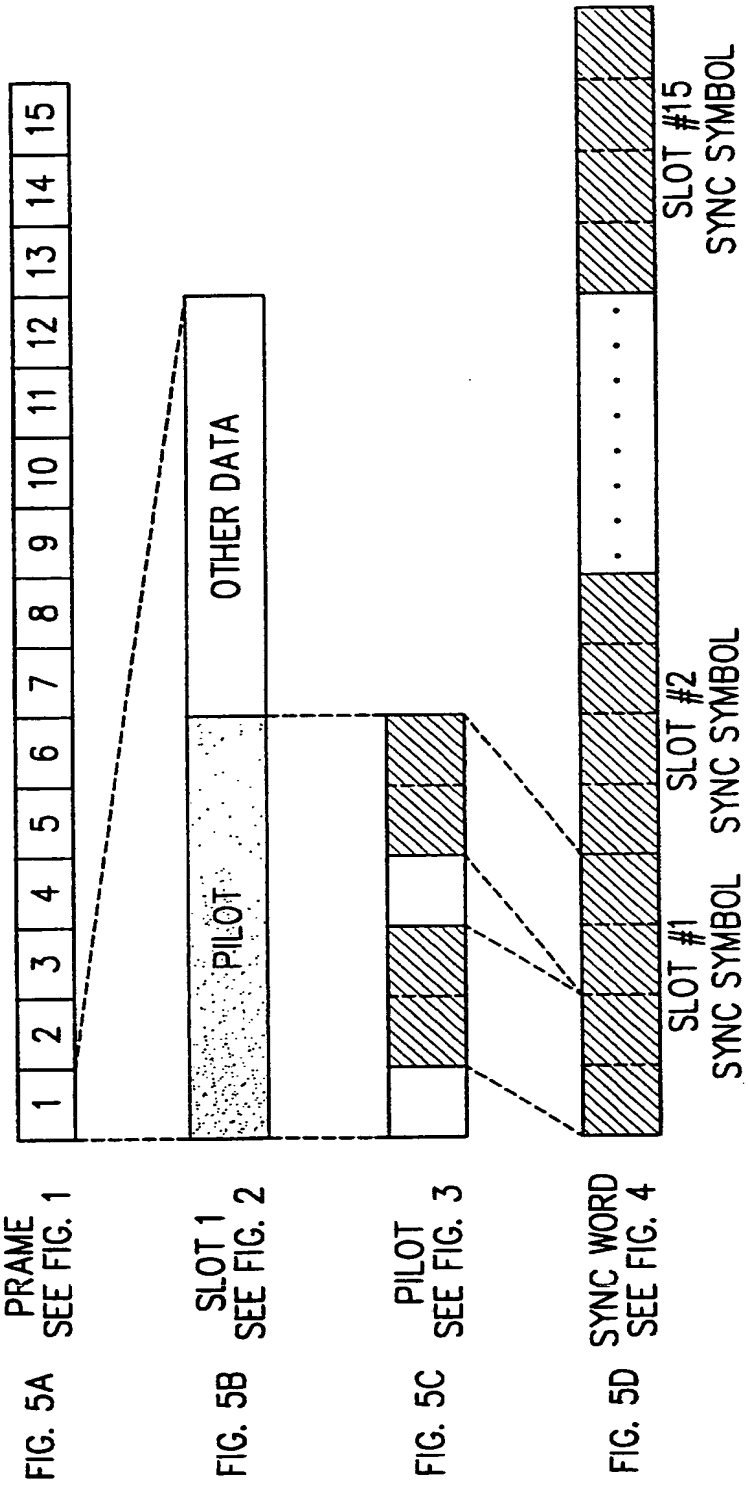
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
PILOT
OTHER DATA
SLOT #1
SYNC SYMBOL
SLOT #2
SYNC SYMBOL
SLOT #15
SYNC SYMBOL
FIG. 5A
PRAME
SEE FIG. 1
FIG. 5B
SLOT 1
SEE FIG. 2
FIG. 5C
PILOT
SEE FIG. 3
FIG. 5D
SYNC WORD
SEE FIG. 4

FIG. 5

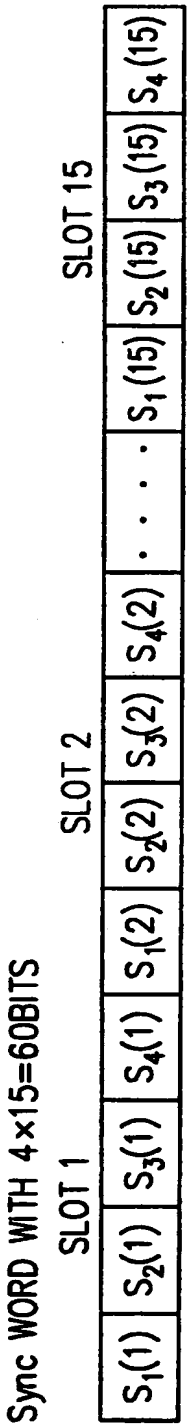
Sync WORD WITH 4×15=60BITS
SLOT 1
SLOT 2
SLOT 15
$S_1(1)$ $S_2(1)$ $S_3(1)$ $S_4(1)$ $S_1(2)$ $S_2(2)$ $S_3(2)$ $S_4(2)$ · · · · $S_1(15)$ $S_2(15)$ $S_3(15)$ $S_4(15)$
$S_n(i)$: i_{th}ELEMENT OF SEQUENCE n

FIG. 6

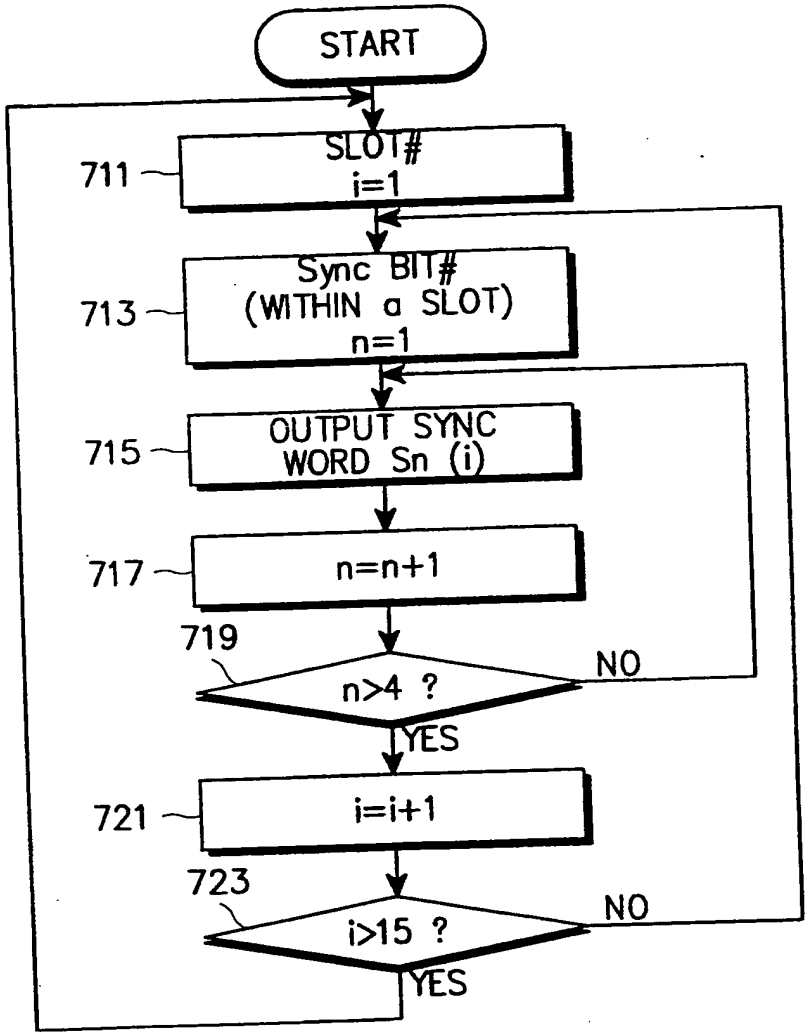
START
711
SLOT#
i=1
713
Sync BIT#
(WITHIN a SLOT)
n=1
715
OUTPUT SYNC
WORD Sn (i)
717
n=n+1
719
n>4 ?
NO
YES
721
i=i+1
723
i>15 ?
NO
YES

FIG. 7

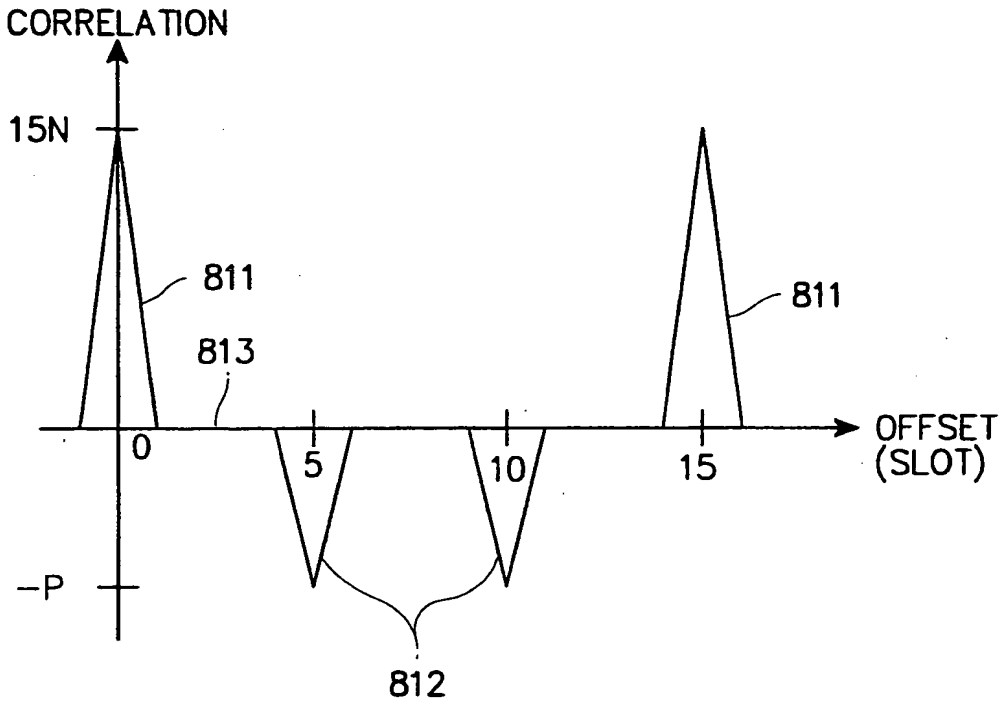

FIG. 8

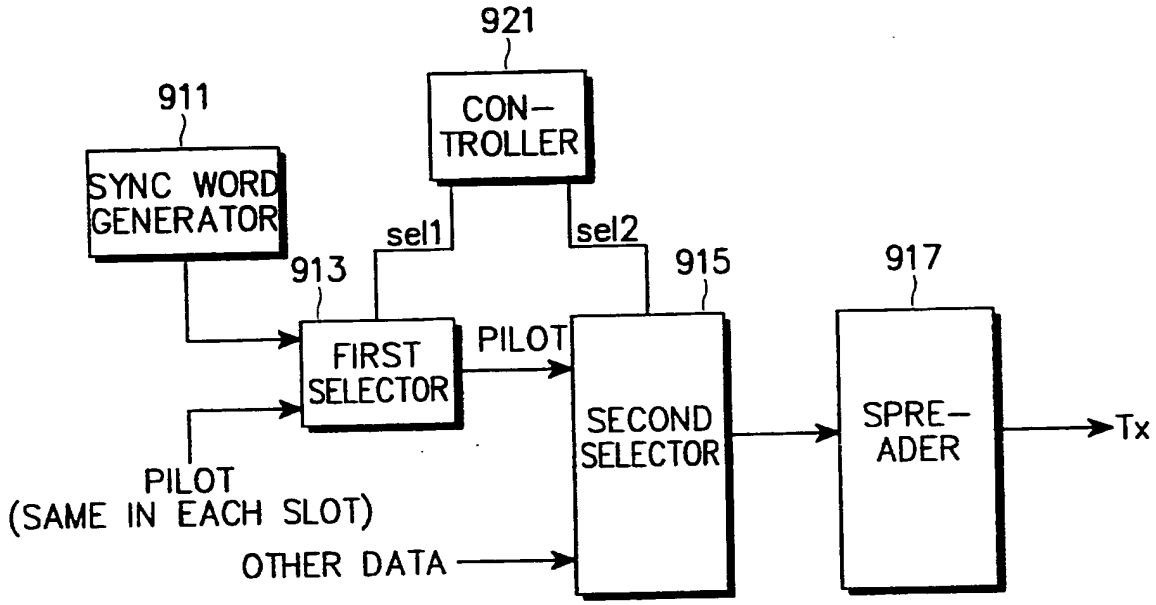
921
911
CON-
TROLLER
SYNC WORD
GENERATOR
sel1
sel2
913
915
917
FIRST
SELECTOR
PILOT
SECOND
SELECTOR
SPRE-
ADER
Tx
PILOT
(SAME IN EACH SLOT)
OTHER DATA

FIG. 9

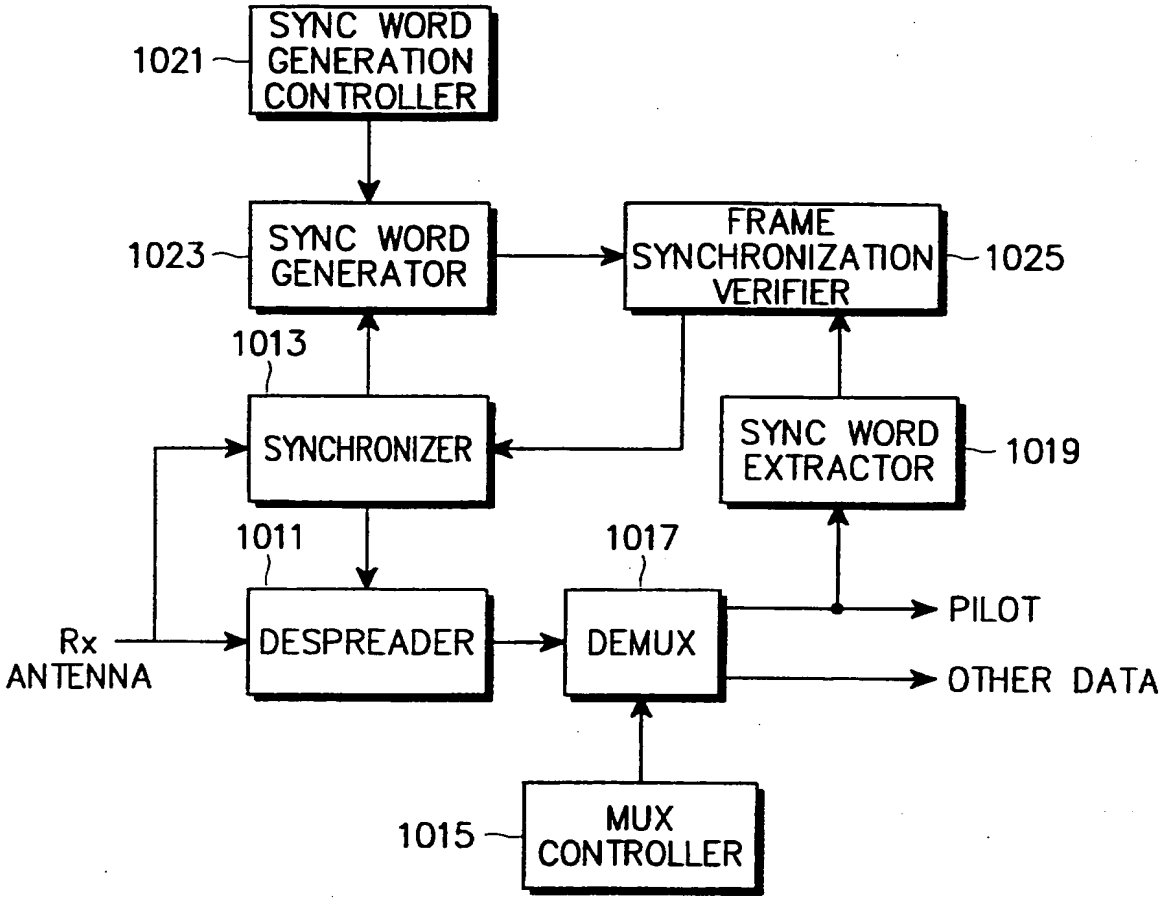
SYNC WORD GENERATION CONTROLLER
1021
SYNC WORD GENERATOR
1023
FRAME SYNCHRONIZATION VERIFIER
1025
1013
SYNCHRONIZER
SYNC WORD EXTRACTOR
1019
1011
1017
Rx ANTENNA
DESPREADER
DEMUX
PILOT
OTHER DATA
1015
MUX CONTROLLER

FIG. 10

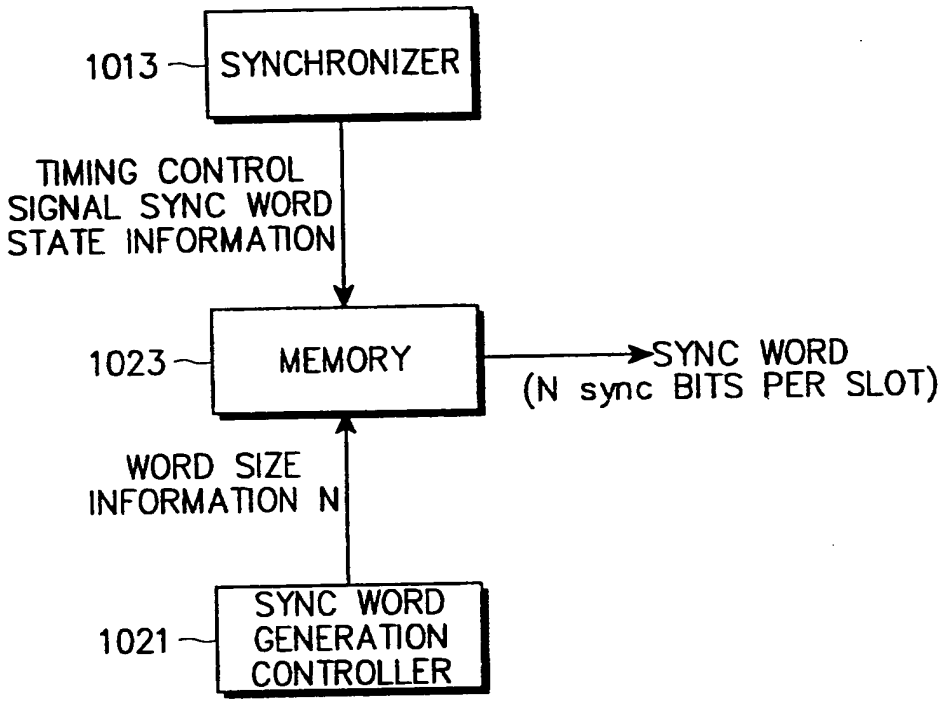
1013
SYNCHRONIZER
TIMING CONTROL
SIGNAL SYNC WORD
STATE INFORMATION
1023
MEMORY
SYNC WORD
(N sync BITS PER SLOT)
WORD SIZE
INFORMATION N
1021
SYNC WORD
GENERATION
CONTROLLER

FIG. 11

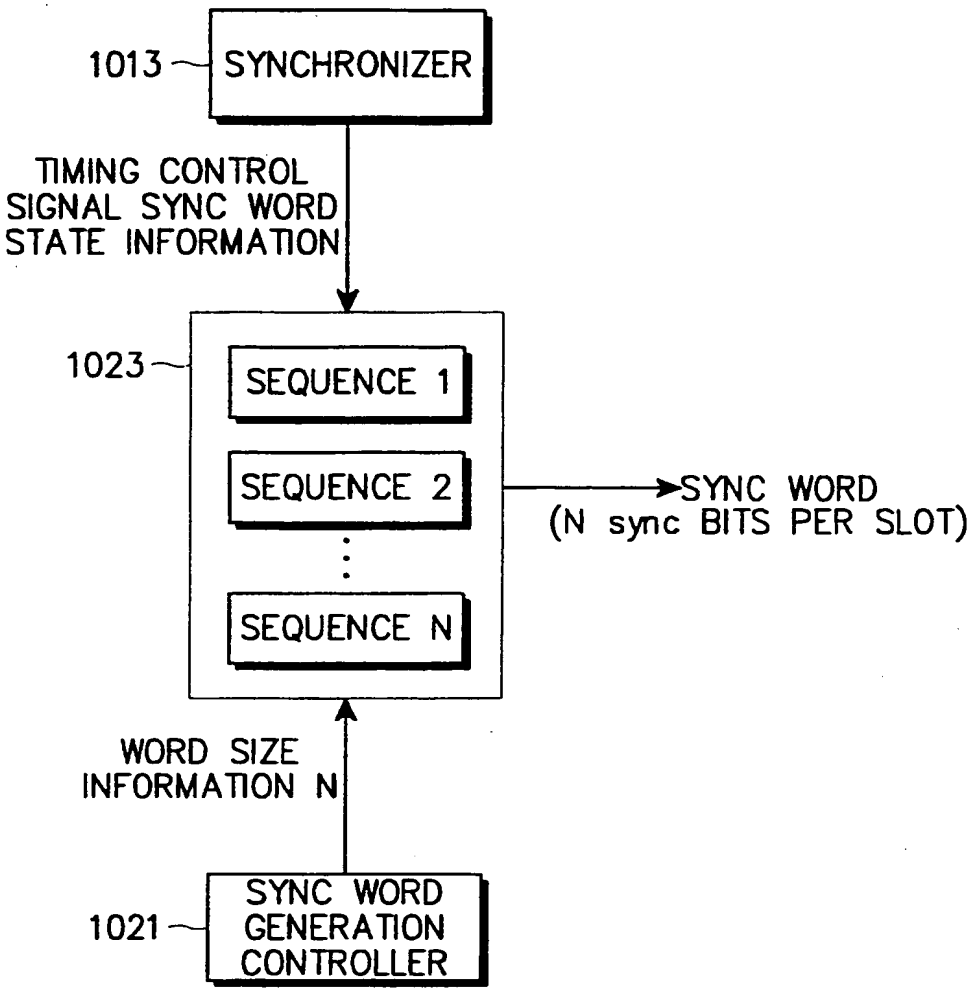
1013
SYNCHRONIZER
TIMING CONTROL SIGNAL SYNC WORD STATE INFORMATION
1023
SEQUENCE 1
SEQUENCE 2
SEQUENCE N
SYNC WORD
(N sync BITS PER SLOT)
WORD SIZE INFORMATION N
1021
SYNC WORD GENERATION CONTROLLER

FIG. 12

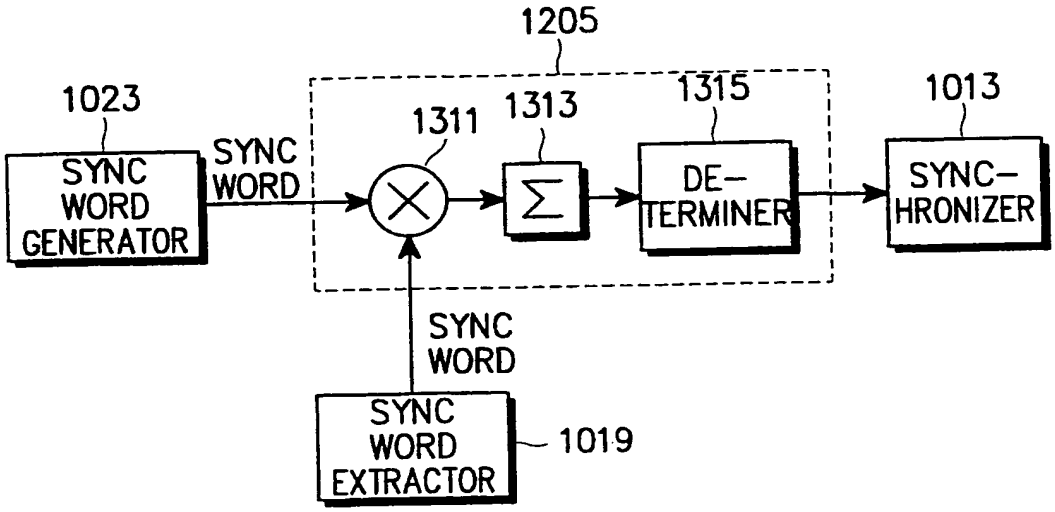

FIG. 13A

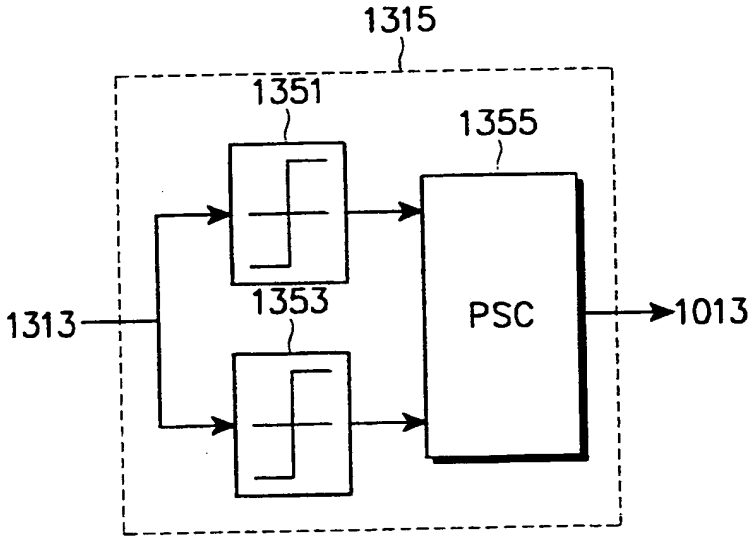

FIG. 13B

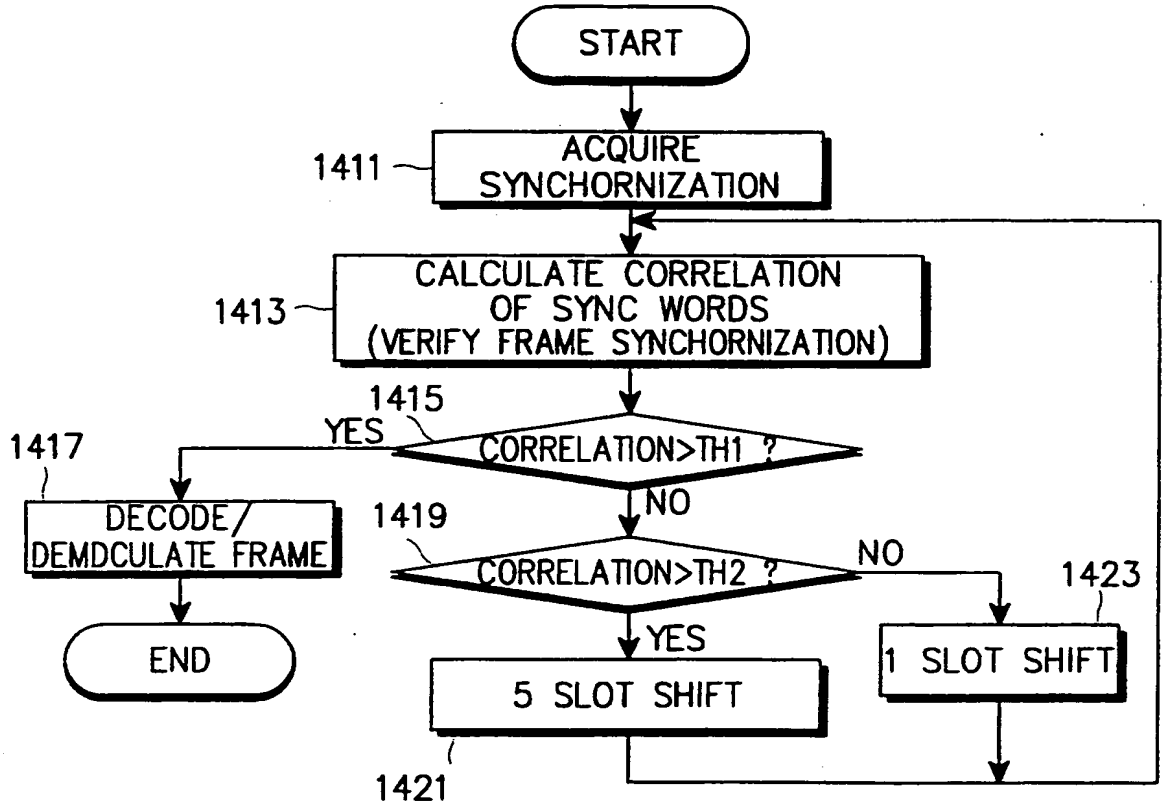
START
1411
ACQUIRE SYNCHORNIZATION
1413
CALCULATE CORRELATION OF SYNC WORDS (VERIFY FRAME SYNCHORNIZATION)
1415
YES
CORRELATION>TH1 ?
1417
DECODE/ DEMDCULATE FRAME
END
NO
1419
CORRELATION>TH2 ?
NO
1423
1 SLOT SHIFT
YES
5 SLOT SHIFT
1421

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR00/00553

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H04J 13/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimun documentation searched (classification system followed by classification symbols)

KE, JP, US, EP classes as above

Documentation searched other than minimun documentation to the extent that such documents are included in the fileds searched

Korean Patents and applications for inventions since 1975
Korean Utility models and applications for Utility models since 1975

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search trerms used)

WPI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 62-91044(KOKUSAI DENSHIN DENWA CO LTD) 25 APRIL 1987 abstract	1 - 24
A	US 4,301,534(DIGITAL SWITCH CORP.) 17 NOVEMBER 1981 abstrach	1 - 24
A	US 5,317,572(FUJITSU LTD) 31 MAY 1994 abstract	1 - 24
A	JP 7-154444(HITACHI DENSHI LTD) 16 JUNE 1995 abstract	1 - 24

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevence
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevence; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevence; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents.such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 SEPTEMBER 2000 (22.09.2000)	25 SEPTEMBER 2000 (25.09.2000)

Name and mailing address of the ISA/KR	Authorized officer
Korean Industrial Property Office Government Complex-Taejon, Dunsan-dong, So-ku, Taejon Metropolitan City 302-701, Republic of Korea Facsimile No. 82-42-472-7140	JEONG, Yong Joo Telephone No. 82-42-481-5674

Form PCT/ISA/210 (second sheet) (July 1998)